IN THE DRAWING:

Please add new Figure 16, attached hereto.

IN THE CLAIMS:

2 ~~152~~. (Amended) The synchronous memory device of claim 1 ~~151~~ further including output drivers, coupled to an external bus, to output data on the bus, in response to the read request, synchronously with respect to an external clock [wherein the value which is representative of the delay time is stored in the register after power is applied to the device].

3 ~~153~~. (Amended) The synchronous memory device of claim [151] 2 ~~152~~ wherein the value [which] is representative of a number of clock cycles of the external clock [the delay time is stored in the register after the memory device is reset].

4 ~~154~~. (Amended) The synchronous memory device of claim 1 ~~151~~ wherein, during an initialization sequence, the programmable register stores the value [which is representative of a delay time is stored in the register when the memory device is initialized].

5 ~~155~~. (Amended) The synchronous semiconductor memory device of claim 1 ~~151~~ wherein, in response to a ~~set register request~~ control register access, the

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programmable register stores the value [which is representative of a delay time is stored in the programmable register].

In claim 157, line 7 insert --a-- before "first."

~~161.~~ (Amended) The synchronous semiconductor memory device of claim ~~157~~ wherein, during an initialization sequence, the programmable register stores the value [which is representative of the programmable delay time is stored in the programmable register after the memory device is initialized].

~~164.~~ (Amended) A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprising:

a programmable register to store a value which is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request [delay time after which the memory device responds to a read request]; and

a plurality of output drivers, coupled to the bus, to output data in response to the read request, wherein the output drivers output data on [a] the bus after the number of clock cycles of the external clock transpire [in accordance with the delay time].

15 ~~165~~. (Amended) The synchronous memory device of claim 14 ~~164~~ wherein the value [which] is representative of a fraction or a whole number of clock cycles of the external clock [the delay time is stored in the register after power is applied to the device].

16 ~~166~~. (Amended) The synchronous memory device of claim 14 ~~164~~ wherein, during an initialization sequence, the programmable register stores the value [which is representative of a delay time is stored in the register when the memory device is initialized].

17 ~~167~~. (Amended) The synchronous semiconductor memory device of claim 14 ~~164~~ wherein, in response to a control register access ~~set register request~~, the programmable register stores the value [which is representative of a delay time is stored in the programmable register].

18 ~~168~~. (Amended) A method of controlling the operation of a synchronous semiconductor memory device wherein the memory device includes a register, the method comprising:

providing a time delay value to the memory device;

storing [a] the time delay [time-delay] value in the register in the memory device, wherein the time delay [time-delay] value is [being] representative of a time delay after which the memory device responds to a transaction request.

Cancel

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In claim 174, on line 1, delete "the step of".

Please **add** the following claims:

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~~177~~. A method of operation of a semiconductor memory device wherein the memory device includes a programmable register, the method comprising:

receiving a time delay value, wherein the time delay value is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request; and

storing the time delay value in the register.

28 27 control

~~178~~. The method of claim ~~177~~ further including receiving a ~~set~~ register access ~~register request~~ wherein, in response to the ~~set register request~~, the register stores the time delay value.

29 28 control register access

~~179~~. The method of claim ~~178~~ further including receiving the ~~set register request~~ and the time delay value in one request packet.

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~~180~~. An integrated circuit device having memory including at least one memory section which includes a plurality of memory cells, the integrated circuit device comprising:

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a programmable register to store a value which is representative of a number of clock cycles of a clock to transpire before data is output onto a bus in response to a read request; and

a plurality of output drivers, coupled to the bus, to output data in response to the read request, wherein the output drivers output data on the bus after the number of clock cycles of the clock transpire and synchronously with respect to the clock.

31 ~~181~~. The integrated circuit device of claim 30 ~~180~~ wherein the value is representative of a fraction or a whole number of clock cycles of the clock.

32 ~~182~~. The integrated circuit device of claim 30 ~~180~~ wherein, during an initialization sequence, the programmable register stores the value.

33 ~~183~~. The integrated circuit device of claim 30 ~~180~~ wherein the integrated circuit device stores the value in the register in response to a control register access ~~set register request~~.